SG2010 PCI-to-StarFabric Bridge

Hardware Implementation Guide

Revision Information: Revision 2.0

Hardware Revision: SG2010-A4

StarGen, Inc., 225 Cedar Hill Street, Suite 22, Marlborough, MA 01752
www.stargen.com

October 2004

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STARGEN

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Introduction

This document serves as a guide for hardware implementation of StarGen's SG2010 PCI-to-StarFabric Bridge device. Implementation requirements will vary based on the specific application.

Overview

This manual contains the following chapters and a glossary,:

Chapter 1 Hardware Description – Provides an overview of the SG2010.

Chapter 2 Power Subsystem Requirements – Defines power and ground requirements.

Chapter 3 Routing and Layout – Discusses transmitter and receiver characteristics.

Chapter 4 CompactPCI and Cable Implementation – Describes serial interface and pin assignments.

Chapter 5 Termination Requirements – Describes pin terminations, reset strap options, and receiver terminations.

Chapter 6 Serial ROM and Parallel ROM – Defines application dependency.

Chapter 7 EMC Considerations – Provides a list of EMC design guidelines

Chapter 8 CompactPCI Hot Swap Requirements – Provides information on the different SG2010 Hot Swap signals.

Chapter 9 LED Usage – Defines modes of operation.

Chapter 10 Example Implementations – Provides implementation details for the different SG2010 configurations.

Chapter 11 Common Implementation Issues – Lists the most common implementation issues in SG2010 designs.

References and Additional Information

If you need additional information, please contact StarGen at support@stargen.com or refer to one or more of the following reference documents:

PCI Special Interest Group (PCISIG) Specifications

PCI Local Bus Specification, Revision 2.2

PCI-to-PCI Bridge Architecture Specification, Rev 1.1

PCI Industrial Computer Manufacturer's Group (PICMG) Specifications

PICMG 2.0 D3.0, CompactPCI Specification

PICMG PCI/ISA Passive Backplane Specification R2.0

PICMG 2.1 R1.0, CompactPCI Hot Swap Specification

PICMG 2.17 StarFabric Specification

StarGen Specifications

SG2010 Hardware Reference Manual

SG2010 Data Sheet

Fabric Programmer's Manual

StarFabric Trade Association Specifications

StarFabric Architecture Specification

Revision History

Revision Number	Date mm/dd/yy	Description
0.0	08/20/01	Preliminary Revision
0.1	05/29/02	Initial Revision
0.2	06/19/02	1. Modified LVDS Routing section. 2. Added additional Power Subsystem details.
0.3	04/23/03	1. LVDS Routing section - removed the 8 inch restriction on LVDS etch lengths 2. Modified SROM section
1.0	07/22/03	1. Added the Example Implementations section 2. Added the Common Implementation Issues section 3. Added the EMI Considerations section 4. Modified the Power Subsystems section - updated the current requirements
2.0	07/19/04	1. Added section 5.7 - REQ Signal Termination

STARGEN 1

Hardware Description

1.1 Description

The PCI-to-StarFabric Bridge (SG2010) device interfaces 64-bit or 32-bit PCI buses operating at 66 MHz or 33 MHz to other StarFabric devices (ex: other SG2010 devices or StarGen's StarFabric Switch, the SG1010). The SG2010 translates PCI traffic into serial frame format for transmission across the switch fabric. By connecting the bridge's serial interface to other bridges or to the StarFabric switch devices, flexible topologies can be designed to fit specific application requirements for bandwidth, reliability, and scalability.

The SG2010 is a multi-function device. The 'bridge' function supports the functionality specified for PCI to PCI Bridges as defined by the PCISIG and provides 100% compatibility with existing PCI software including configuration, BIOS, OS, and drivers. The 'gateway' function provides StarFabric-native path routing and multicast routing capability and other enhanced features.

The fabric interface consists of two 2.5Gbps full duplex links providing 2.5Gbps bandwidth simultaneously in each direction. Four aggregated 622Mbps LVDS differential pairs in each direction are used to create the 2.5Gbps link. The two links can be bundled to create a 5Gbps full duplex port to another device or can be used separately for redundant connections.

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Power Subsystem Requirements

2.1 Power Sub-System Overview

In determining the layer stack in printed circuit board (PCB) design, it is important to consider the power and ground requirements first. To help control transmission line impedances it is recommended that multi-layer board structures be used with solid uniform power and ground planes. Routing signals over partial planes will cause impedance discontinuities and decrease signal quality. Using solid planes also improves the power distribution for the board. It may be helpful to stack power and ground planes next to each other as this forms a parallel plate capacitor that aids in filtering power supply noise. Reducing the separation between these two planes increases the capacitance between them. Common ground planes should be connected with numerous via to help ensure good current return flow.

2.2 Power and Ground Planes

The SG2010 requires +3.3V for I/O and +1.5V for core, CDR, and PLL power. Separate power/ground plane pairs are recommended for the IO and core voltages. Partial planes or wide etch are recommended for both the PLL and CDR power. Power and ground plane splits should be avoided, but if a split is used, avoid routing high-speed signals (Ex. LVDS) over it. Several high-frequency capacitors should be placed across plane splits to provide a return path for common mode AC current.

2.3 Voltage Regulation

The SG2010 requires two supplies 3.3V and 1.5V. The 1.5V supply is split up into three different references V15 (power for the core), VDDG (power for the 78Mhz PLL), and VDDA (power for the Link interface). The 3.3V supply (V33) provides the power for the I/O interface of the SG2010. The maximum current requirements for each of the reference voltage are listed below:

- 1.5V = 342 mA
- 3.3V = 479 mA

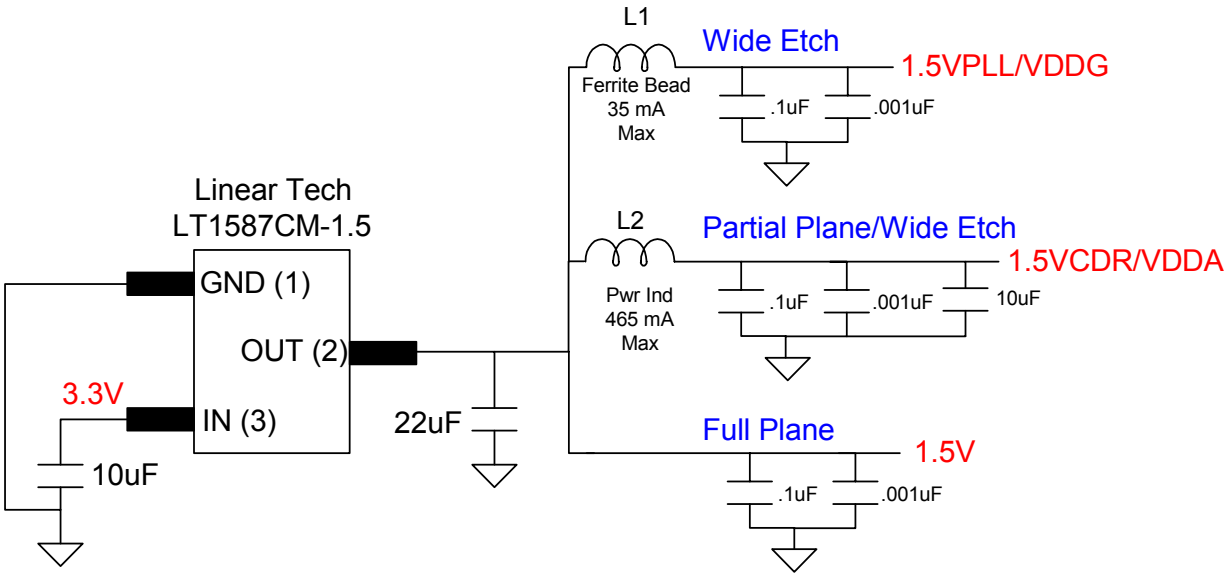
These numbers were taken with the following testing parameters

– Maximum loading: 10 Loads at 33 Mhz/64 Bit

– Maximum temperature: 85 degrees C
– Fastest Process: SG2010 A4 Fast

An adequate supply or voltage regulator circuit must be provided for each voltage 1.5V and 3.3V. Many system platforms provide an adequate 3.3V source. If a 1.5V supply is not available, it can be derived from the 3.3V supply with a simple regulator circuit as shown in Figure 2–1. The full plane (1.5V) should be connected to the V15 pins and the partial planes or wide etch, 1.5VCDR and 1.5VPLL, should connect to the VDDG and VDDA pins respectively. Careful consideration should be taken when choosing the inductors required for the circuit. The inductors need to be able to handle the current required by each reference.

Figure 2–1 1.5 Voltage Regulator Circuit



Example Inductors		
Ind	Vendor	Vendor _PN
L1	Coilcraft	0603CS-R12X_BC
L2	Coilcraft	DS1608C-222

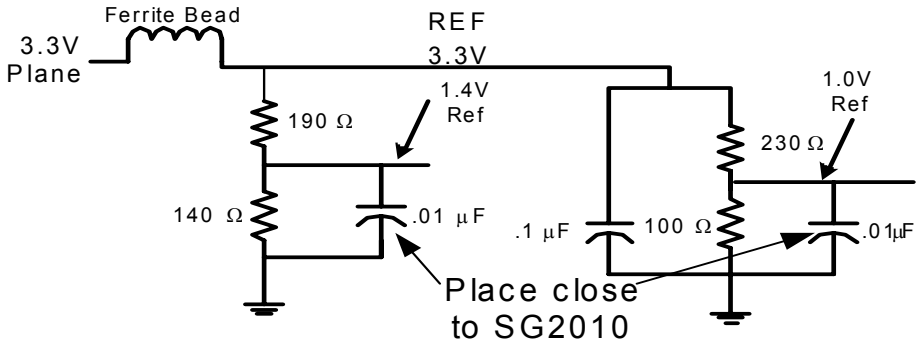
If an implementation requires a 1.5V supply for multiple devices, a switching regulation circuit may be needed to supply the necessary current. For SG2010 designs that require only a few SG2010's, Linear Technology's LT1587CM-1.5 has been successfully used. Refer to vendor data sheets for specific implementation guidelines for the selected regulator.

2.4 Voltage Reference Requirements

2.4.1 LVDS Transmitter Reference

In addition to the +3.3V and +1.5V supplies, the SG2010 requires reference voltages for the LVDS transmitters. These are nominally 1.0Vdc and 1.4Vdc values applied to the REF10 (BGA location B8) and REF14 (BGA location A8) input pins respectively. It is acceptable to derive these from other supplies using a resistor divider network as shown in Figure 2–2. It is important to provide stable and clean power for these references to minimize noise. A choke circuit for the divider is recommended. High-frequency decoupling of 0.01uF should be placed as close to the SG2010 REF10 and REF14 device pins as possible, and the circuit should be connected to the reference pins with wide low impedance copper etch. See Figure 2–2 for more details.

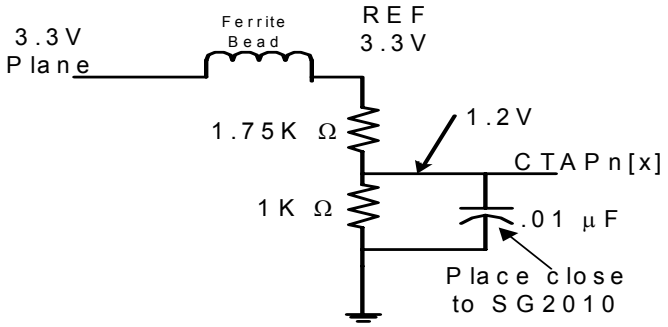
Figure 2–2 REF10 and REF14 circuit



2.4.2 LVDS Receiver Reference

If AC-coupling is used at the SG2010 receivers, a Vcommon Recovery circuit will be required to re-establish the DC reference for the differential signals at the SG2010. This voltage is nominally 1.2V and can also be derived with a resistor divider network (from the +3.3V or +1.5V supplies). The SG2010 has eight CTAP pins (4 CTAP pins per link). To help save board real estate and reduce the part count, the four CTAP within a link can be grouped together to a circuit similar to the one shown in Figure 2–3. If SG2010 receivers are DC coupled the CTAPn[x] pins should be tied to a .01uF cap to ground.

Figure 2–3 Vcommon Recovery Circuit



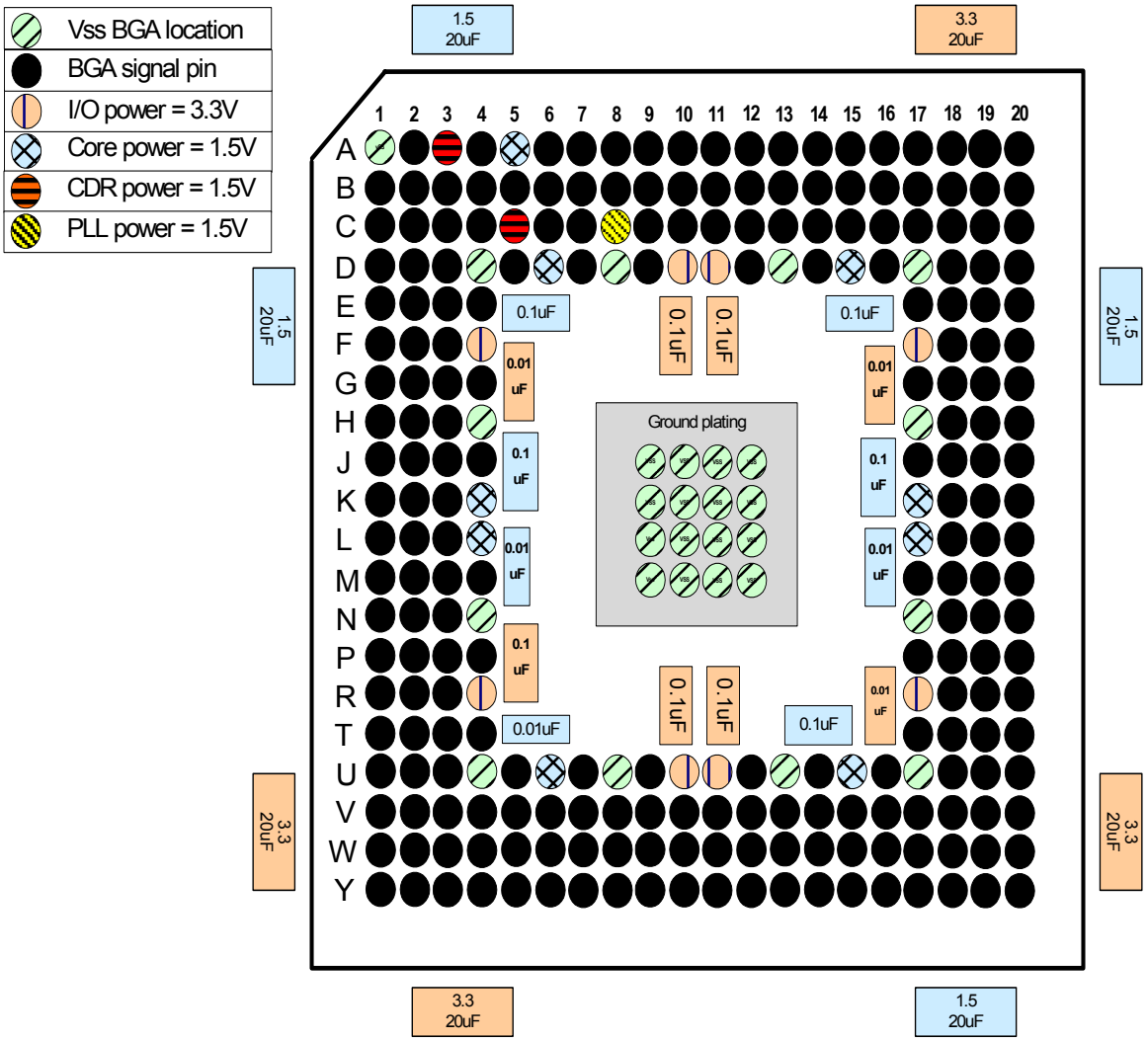
2.5 Decoupling

Good power decoupling for all active components is necessary. A combination of bulk capacitance and the use of high-frequency, low inductance local capacitance for each IC are recommended. The bulk decoupling capacitors should be distributed evenly over the board for each supply. The high-frequency capacitors should be placed as close as possible to the power pins that they are decoupling.

2.5.1 SG2010 Decoupling

Local low inductance, high frequency capacitors should be placed as close as possible to the SG2010 for each power/ground pin pair. Bulk capacitors should also be used to provide stable 3.3V and 1.5V references for the SG2010. Figure 2–4 depicts a typical design with the capacitors on the opposite side of the PCB from the SG2010.

Figure 2–4 Typical Decoupling for SG2010



2.5.2 PCI Decoupling

For PCI expansion board applications, an average capacitance of 0.047µF should be used for each pin labeled VI/O. The +3.3V, +5V, and any unused VI/O power pins need to be decoupled to ground with a minimum average capacitance of 0.01µF per pin in order to provide an AC return path for PCI bus signals. Use of ceramic chip capacitors made with an X7R or BX dielectric is recommended. Pins may share the same capacitor as long as the trace length from the capacitor pad to the connector pin pad doesn't exceed 0.25 inches. This trace must also have a minimum trace width of 20 mils. It is highly recommended to have a bulk decoupling capacitor at the power entry point for each voltage on the circuit board. A suitable capacitor is a 10µF (or higher) tantalum capacitor with a low equivalent series resistance (ESR). These capacitors should also be placed within 0.25 inches of the board's edge connector. To avoid overstressing, use capacitors with voltage ratings approximately three times the nominal working voltage. Please see the PCI Specification for more details.

2.5.3 CompactPCI Decoupling

CompactPCI boards must meet the same decoupling requirements as PCI boards. In addition, high frequency 0.1µF ceramic capacitors must be added to each supply voltage (+3.3V, +5V, +/-12V, VI/O) on the J1 and J2 connectors. One capacitor must be used for every 10 power pins. If a hot swap conntroller is implemented on the board, bulk capacitance should not be placed on the voltage pins from J1. All bulk capacitance should be connected to the voltages generated after the hot swap controller. Please see the Hot Swap specification for more details.

STARGEN 3

Routing and Layout

3.1 Routing Overview

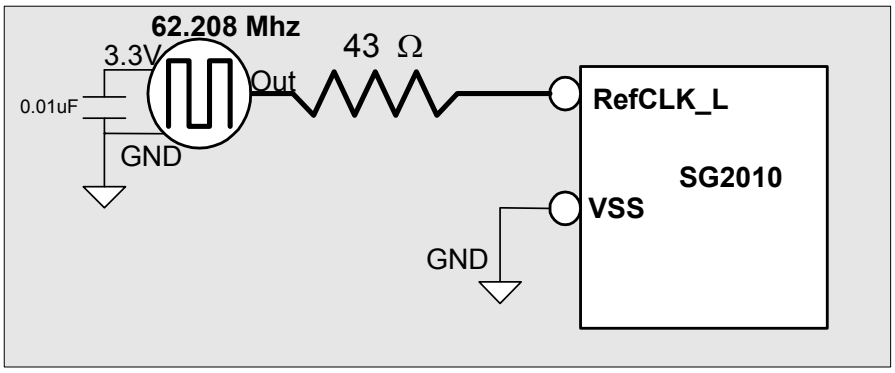
The use of signal traces with sharp 90° or greater turns should be avoided because this is a source of impedance discontinuity at high frequencies. Using chamfered turns or 45° bends are recommended alternatives. Components that terminate to a power plane, such as bypass capacitors connecting to ground, should keep their traces as short as possible for a low impedance connection.

3.2 Oscillator Requirements

The SG2010 has an on-chip phase locked loop (PLL) that is used for the clock and data recovery (CDR) of the serial transmissions. An external 62.208 MHz crystal oscillator is required for operation. This clock source should be placed close to the SG2010 IC's REFCLK_L input pin (B3) to reduce radiated noise from the components and the connecting etch. The frequency deviation should not exceed 25ppm, and the peak to peak jitter should not exceed 100ps.

A series damping resistor between the oscillator and SG2010 REFCLKL pin is recommended to create a source terminated transmission line. It is also recommended that a high frequency bypass capacitor be placed between the power and ground pins. The designer may consider using a more robust power supply filtering circuit, such as a choke circuit (not shown in example), for the oscillator. See Figure 3–1 for an example circuit.

Figure 3–1 Oscillator Routing



3.3 LVDS Routing

3.3.1 LVDS Serial Transmitter and Receiver Characteristics

The serial transmitters and receivers used in StarGen devices are compatible with the TIA/EIA-644 and IEEE 1596.3 LVDS specifications. They transfer data at a 622Mbps rate with a loop current between 2.5mA and 4.5mA. Each transmitter has on-chip termination to minimize reflections and improve signal integrity across backplanes and connectors. Each receiver has an internal 100Ω nominal resistor that provides the required impedance to produce a voltage across the receiver. This voltage is typically 400mV with a center point at +1.2V. The receiver provides +/- 100mV sensitivity over a common-mode range of 0V to 2.4V and compensates for skew between differential pairs for proper detection. The LVDS pairs may be AC coupled. If they are, a Vcommon recovery circuit is required at the receiver end to properly restore a DC value.

3.3.2 LVDS Transmission Lines

Because of the low voltage swing and high-speed nature of LVDS, special attention must be paid to these signals. Due to the LVDS routing requirements, it is recommended that LVDS routing be completed before CMOS or TTL signals. On a circuit board, each differential signal pair should have its traces routed as close to each other as possible once they leave the IC package to produce a tightly coupled transmission line.The maximum recommended skew between the + and - signals *within* each differential pair should be no more than 25ps.

Tight control of etch length *between* pairs in a link is not necessary, but significant differences should be avoided. StarGen recommends a maximum time skew of 300ps between the four differential pairs that comprise an SG2010 link. Figure 3–2 shows the LVDS skew requirements for one SG2010 link.

Figure 3–2 LVDS Skew Requirements

The LVDS portion/layers of the circuit board must be constructed with controlled transmission line impedance of 50Ω (100Ω differential). Trace impedance should be controlled within +/- 10%, but +/- 5% control is recommended. To accomplish this, either microstrip or stripline fabrication technique can be used.

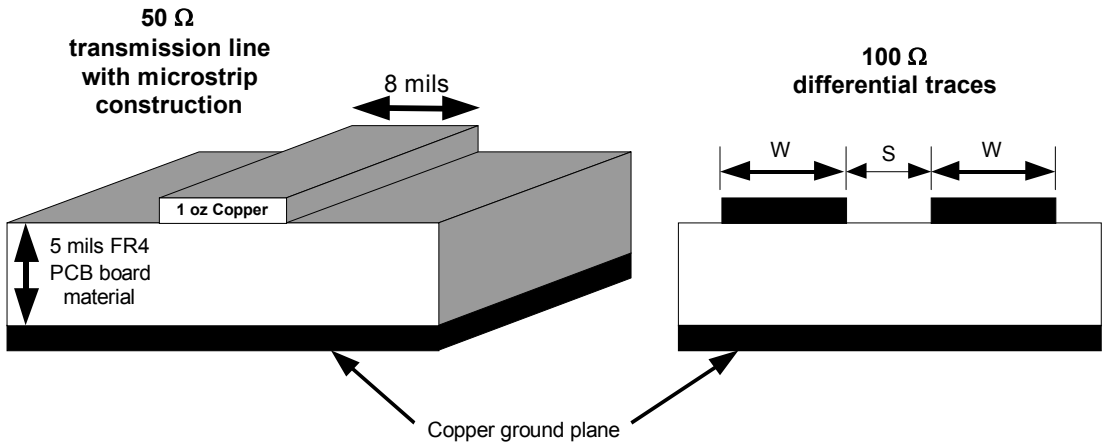
StarGen recommends the use of separate PCB layers for LVDS signals if possible. If the LVDS is routed on the same layer as digital CMOS or TTL signals, then a minimum distance of ~30 mils should be maintained between the digital signals and the LVDS signals.

3.3.3 LVDS Routing Options

3.3.3.1 Microstrip LVDS Routing

Microstrip transmission lines (Figure 3–3) are created when signal traces are routed on an outer layer of a printed circuit board over a ground plane.

Figure 3–3 Microstrip Transmission Line



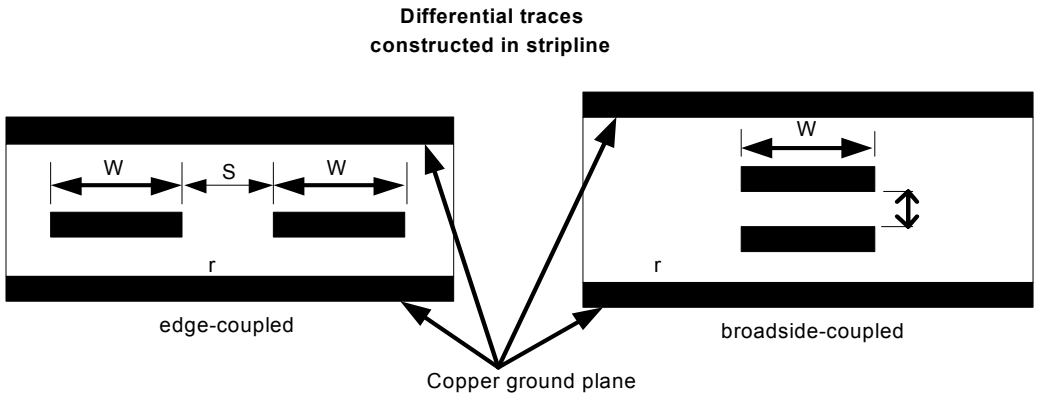
Two single-ended 50Ω transmission lines need to be constructed in PCB etch for each LVDS differential pair. Line to line spacing between the differential signals should be less than the dielectric thickness separating the traces from their reference plane (which is less than 5 mils for the microstrip example above). A line to line spacing between 1 to 3 mils is recommended. To design the 100Ω differential impedance, the width of the

traces should be adjusted appropriately. An advantage of microstrip construction (Figure 3–3) is that it is possible to route traces directly from a source pin to a destination without the need of vias. Minimizing the number of vias is important for maintaining good signal quality. A disadvantage with microstrip is that it can limit the number of routing channels on a circuit board.

3.3.3.2 Stripline LVDS Routing

Stripline (Figure 3–4) is constructed by routing traces on an inner layer between two reference planes (power or ground).

Figure 3–4 Stripline Transmission Line



Traces can be edge coupled (side-by-side), or broadside coupled (one above the other). Stripline provides additional shielding that helps to reduce noise coupling onto the signal lines and aids in limiting radiation. However, inner layer signals require the use of vias and typically add layers to the circuit board. Stripline also slows down a signal's propagation velocity. Broadside constructed stripline increases the number of available routing channels at the cost of a more complex fabrication process.

For either construction technique, the distance *between* differential pairs should be a minimum of 2S, where “S” is the spacing between the positive and negative sides of a differential pair. 20 mil separation or more is recommended if there is sufficient room. Also, the differential signals should be routed over a continuous uniform power plane. Vias and stubs should be minimized/avoided.

3.3.4 Summary of LVDS Routing Recommendations

The following list summarizes the LVDS routing recommendations:

- The distance *between* differential pairs should be a minimum of 2S. 20 mil separation or more is recommended.
- The LVDS portion/layers of the circuit board must be constructed with controlled transmission line impedance of 50Ω (100Ω differential).
- Trace impedance should be controlled within +/- 10%, but +/- 5% control is recommended.

- A minimum distance of ~30 mils should be maintained between the digital signals and the LVDS signals.
- The maximum recommended skew between the + and - signals *within* each differential pair should be no more than 25ps.
- StarGen recommends a maximum time skew of 300ps between the four differential pairs that comprise an SG2010 link.
- LVDS routing should be completed before digital CMOS and TTL routing.

STARGEN 4

CompactPCI and Cable Implementation

4.1 Implementation Choices for CompactPCI Cards

There are several implementation choices for interfacing the SG2010 on a CompactPCI card. These include options that are compliant with the PICMG 2.17 StarFabric specification, applications that route PCI to the J1/J2 cPCI connectors for System Slot, Peripheral slot or mixed System/Peripheral slot use, and implementations that route to and from PMC carrier sites on cPCI cards.

4.1.1 PICMG 2.17 Node Board Requirements

For PICMG 2.17 node board applications, the SG2010 StarFabric LVDS interface is routed from the J3 cPCI connector and the SG2010 PCI interface is either (1) local to the cPCI board, (2) routes to the cPCI J1/J2 connectors or (3) routes to the PMC connector on the cPCI board. The pin assignments for the J3 connector are contained in the PICMG 2.17 StarFabric specification. Table 4–1 provides a copy of one of the PICMG 2.17 J3 pin assignment choices. Refer to the PICMG 2.17 StarFabric specification for more details and options.

As Table 4–1 shows, PICMG 2.17 StarFabric LVDS signal mapping utilizes one row of a CompactPCI connector for two differential pairs. One of these differential pairs is used for Tx+ and Tx- signals; the second is used for Rx+ and Rx- signals. With this mapping, a single full-duplex StarFabric link (four differential pairs in each direction) uses four rows on a CompactPCI connector.

Table 4–1 Example PICMG 2.17 LVDS Mappings on J3

Row							
19	GND	GADDR	GADDR	GADDR	GADDR	GADDR	GND
18	GND	GND	GND	GND	GND	GND	GND
17	GND	L3_Tx3+	L3_Tx3-	GND	L3_Rx3+	L3_Rx3-	GND
16	GND	L3_Tx2+	L3_Tx2-	GND	L3_Rx2+	L3_Rx2-	GND
15	GND	L3_Tx1+	L3_Tx1-	GND	L3_Rx1+	L3_Rx1-	GND
14	GND	L3_Tx0+	L3_Tx0-	GND	L3_Rx0+	L3_Rx0-	GND
13	GND	L2_Tx3+	L2_Tx3-	GND	L2_Rx3+	L2_Rx3-	GND
12	GND	L2_Tx2+	L2_Tx2-	GND	L2_Rx2+	L2_Rx2-	GND
11	GND	L2_Tx1+	L2_Tx1-	GND	L2_Rx1+	L2_Rx1-	GND
10	GND	L2_Tx0+	L2_Tx0-	GND	L2_Rx0+	L2_Rx0-	GND
9	GND	L1_Tx3+	L1_Tx3-	GND	L1_Rx3+	L1_Rx3-	GND
8	GND	L1_Tx2+	L1_Tx2-	GND	L1_Rx2+	L1_Rx2-	GND
7	GND	L1_Tx1+	L1_Tx1-	GND	L1_Rx1+	L1_Rx1-	GND
6	GND	L1_Tx0+	L1_Tx0-	GND	L1_Rx0+	L1_Rx0-	GND
5	GND	L0_Tx3+	L0_Tx3-	GND	L0_Rx3+	L0_Rx3-	GND
4	GND	L0_Tx2+	L0_Tx2-	GND	L0_Rx2+	L0_Rx2-	GND
3	GND	L0_Tx1+	L0_Tx1-	GND	L0_Rx1+	L0_Rx1-	GND
2	GND	L0_Tx0+	L0_Tx0-	GND	L0_Rx0+	L0_Rx0-	GND
1	GND	GND	GND	GND	GND	GND	GND
	Z	**A**	**B**	**C**	**D**	**E**	**F**

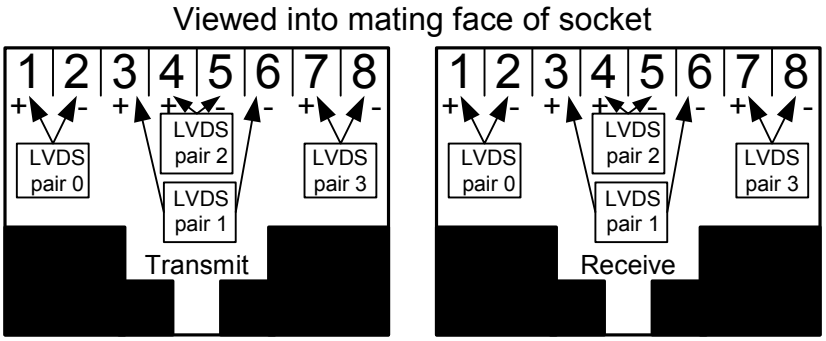
4.2 Cable Implementation

For cable applications, the LVDS serial interface on the SG2010 can be connected using a variety of interconnect choices. RJ45 connectors and cable recommendations are described below.

4.2.1 RJ45 LVDS Pin Assignments

If RJ45 connectors (Figure 4–1) are used for cable interconnect, one connector should be used for the four transmit differential pairs in a link. A second RJ45 should be used for the four receive differential pairs in a link. To help save board real-estate, dual RJ45 connectors can also be used. The pin assignments for RJ45 transmit and receive differential pairs are shown in Figure 4–1.

Figure 4–1 RJ45 LVDS Pin Assignment



4.2.2 CAT5 Use Guidelines

Cable interconnect can be accomplished with Category 5E cable up to **40 feet** in length. This length may be reduced, dependent upon the cable quality or type. When cable is used to connect chassis with different ground potential, AC-coupling for the LVDS receivers is recommended. AC termination implementation and re-establishment of the DC Vcommon voltage on the LVDS receiving node is discussed in Section 5.6.

STARGEN 5

Termination Requirements

5.1 Pin Terminations

5.1.1 Factory Test Signal Termination

The Signals listed in Table 5–1 are not required for SG2010 applications. They are internally terminated and should be left as NO CONNECTS for all applications.

Table 5–1 Signals Terminated with NO CONNECT

Signal Name	BGA	External Termination
tstshftld	B1	No-connect
ecsel	C2	No-connect
etoggle	D2	No-connect
exdnup	D3	No-connect
tstphase	E4	No-connect
scan_ena	L3	No-connect
testrst	A20	No-connect
tstclkl	C4	No-connect
bypassl	B2	No-connect
resettx	A2	No-connect
loopbken	C3	No-connect
reserved[4]	G2	No-connect
reserved[2]	H3	No-connect
reserved[1]	H2	No-connect
reserved[0]	H1	No-connect

5.1.2 JTAG

If the JTAG interface is not being used, it is recommended that the TRST_L signal be pulled down with a 10kΩ resistor. For designs that use more than one StarFabric device (SG2010 or SG1010), designers should be aware that each device has an internal 50 K ohm pull-up resistor and a stronger pull-down should be used on TRST_L. If the SG2010 TRST_L signal is not pulled down, the SG2010 will operate normally but the JTAG interface is active. When the JTAG interface of the SG2010 is accessed, normal chip operation is not guaranteed.

If JTAG is implemented on the board, the SG2010 JTAG signals should be connected to the appropriate PCI connector pins or connected appropriately to complete the JTAG chain with other devices.

Table 5–2 Recommended JTAG Pin Terminations

Signal Name	BGA	External Termination
trst_l	V2	10k Ω Pulldown
tck	W1	No-connect
tms	V3	No-connect
tdi	Y1	No-connect

5.1.3 Other Test Pin Termination Requirements

Table 5–3 provides termination requirements for the TESTMODE[3:0] and TSTCLKG signals. Use of these signals is optional. If not used, they should all be terminated as shown in the table. If it is desireable to control Testmode features for an application, then TESTMODE[3:0] can be tied to a DIP switch or an option can be provided to pull one or more of these pins to 3.3V via a strapping resistor. For normal operation, they should all be pulled to GND. The TSTCLKG signal can be left as a NO CONNECT. If the capability of running the SG2010 in PLL Bypass mode is desired, it can be connected to a 77.76Mhz oscillator through a series termination resistor of ~40 Ω. The PLL Bypass mode is required for thermal evaluation above 70 degrees C. The SG2010 is put in PLL bypass mode by setting testmode[0] to a logic high and testmode[1:3] to a logic low.

Table 5–3 Recommended Test Pin Terminations

Signal Name	BGA	External Termination
trst_l	V2	10k Ω Pulldown
tck	W1	No-connect
tms	V3	No-connect
tdi	Y1	No-connect
tstclkg	C18	No-connect
testmode[3]	H18	10k Ω Pulldown

Table 5–3 Recommended Test Pin Terminations

Signal Name	BGA	External Termination
testmode[2]	G20	10k Ω Pulldown
testmode[1]	G18	10k Ω Pulldown
testmode[0]	F20	10k Ω Pulldown

5.2 Reset Strap Options

Several SG2010 features are enabled or disabled at reset with strapping pins. Pins can be pulled up/down for fixed settings or can be controlled with Dip switches, FETs or strapping resistors if flexibility is required. Refer to Table 5–4 for reset strapping options and to the *SG2010 Hardware Reference Manual* for additional information.

Table 5–4 Reset Strapping Options

Signal	Function if pulled LOW	Function if pulled HIGH	Alias Name
LEDHM	Differential pair state is driven on LEDx[3:0] for all 4 differential pairs within each link.	Link state is driven only on LEDx[0] for each link	PR_AD[3]
PFN0	If a Root, sets the Fabric ID to 0/0/7777777.	If a ROOT, sets the Fabric ID to 1/0/7777777.	PR_AD[4]
LOCKOUT	SG2010 responds normally	SG2010 responds with Lockout status	PR_AD[5]
ARBEN	Arbiter disabled	Arbiter enabled	PR_AD[6]
CFEN	SG2010 does NOT perform central functions during Reset	SG2010 DOES perform central functions during Reset	PR_AD[7]
ROOT	Configured as a Leaf	Configured as a Root	
BRIDGE_EN	PCI -PCI Bridge function disabled	PCI -PCI Bridge function enabled	

The SG2010 also has pins that are used for cPCI Hot Swap. These pins must be terminated appropriately according to the application. The reset value of SKIPINS is established by sampling PR_AD2. Table 5–5 provides a brief description of each pin and how the pin must be terminated in a Non-Hot Swap environment.

Table 5–5 cPCI Hot Swap Signals

Signal	Description	External Terminations
BDSEL_L	CompactPCI Hot Swap board seated. When sampled high, the SG2010 does not respond to or initiate any PCI transactions (after completing any ongoing transactions). When sampled low, the SG2010 responds to and initiates PCI transactions normally.	10k Ω Pulldown
ENUM_L	CompactPCI Hot Swap interrupt. The SG2010 can be enabled to sample this signal and forward it through the event dispatcher, and can be enabled to assert this signal when it receives an event directed to the ENUM_L EMU address.	10k Ω Pull-up
L64EN_L	CompactPCI Hot Swap local 64-bit extension enable. When the SG2010 samples this signal low, it enables the PCI 64-bit extension signals. When the SG2010 samples this signal high, the PCI 64-bit extension signals are only enabled if REQ64_L is sampled low during RST_L or LRST_L.	10k Ω Pull-up
LSTAT	CompactPCI Hot Swap ejector handle switch status. Sampled by the SG2010 to determine when the ejector handle switch is open or closed, controlling the hot swap state machine. When a 1, the ejector handle is open. When a 0, the ejector handle is closed.	10k Ω Pulldown
SKIPINS (PR_AD[2])	When 1, enables the hot swap controller to skip insertion state after power up. It does not effect re-insertion after removal. When 0, the hot swap controller goes through the insertion state as specified in the CompactPCI Hot Swap specification.	10k Ω Pull-up

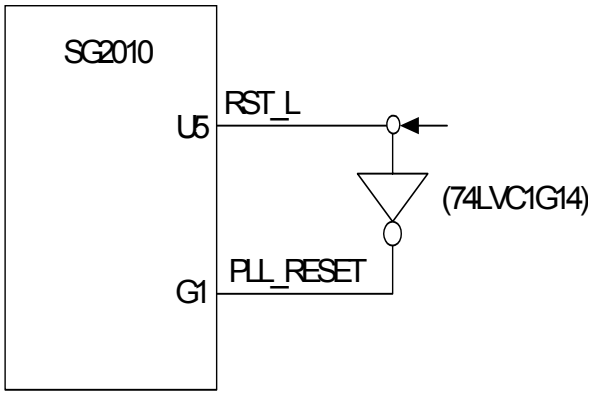
5.3 LVDS 100 Ohm Reference

The RESHI and RESLO pins on the SG2010 must be connected to each other through a 100Ω, 1% resistor. This is used for LVDS termination reference.

5.4 PLL Reset Signal Implementation

The PLL_reset signal (BGA location G1), requires an inverter circuit to assure that the on-chip PLL resets properly. An example circuit is shown in Figure 5–1.

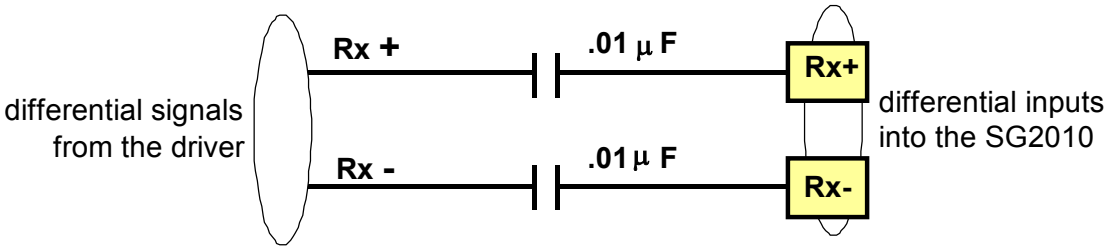
Figure 5–1 PLL Reset Circuit



5.5 Optional AC-Coupling for LVDS Receivers

AC-coupling at the LVDS receivers is recommended for cable applications and those where there may be a difference in ground potential between the sending and receiving SG2010 (or other StarFabric devices). To accomplish this, a 0.01µF series capacitor must be placed in series with each of the Rx+ and Rx- signal pins on the SG2010. The exact location is not important, but placement close to the connector relieves congestion around the SG2010.

Figure 5–2 AC-Coupling



5.6 LVDS Receiver Termination

The SG2010 device provides a center-tap pin for each LVDS receiver pair. These eight signals are labeled CTAP0[3:0], CTAP1[3:0]. Each pin can be individually tied to ground with a 0.01µF capacitor or a single 0.01µF capacitor can be shared for the four differential pairs in a link to save PCB real estate. If AC-termination is used at the SG2010 LVDS receivers, a Vcommon recovery voltage must also be applied to the CTAP input signals. This is nominally +1.2Vdc. An example circuit is shown in Figure 2–3.

5.7 REQ Signal Termination

All of the request signals of the SG2010 require an external pull-up. If the arbiter of the SG2010 is disabled REQ_L[1:8] can all be connected to a single ~10K pull-up, with REQ_L[0]/AGNT_L connected to its own pullup. If the arbiter is enabled an individual pullup (10K-100K) is required on each REQ signal.

Table 5–6 REQ Signal Termination

Signal	External Termination
REQ_L[0]/AGNT_L	~10K-100K Ohm Res
REQ_L[1:8]	Arb Dis - All pins can be connected to one ~10K Ohm Res Arb Ena - Each signal should have an individual ~10K-100K Ohm Res

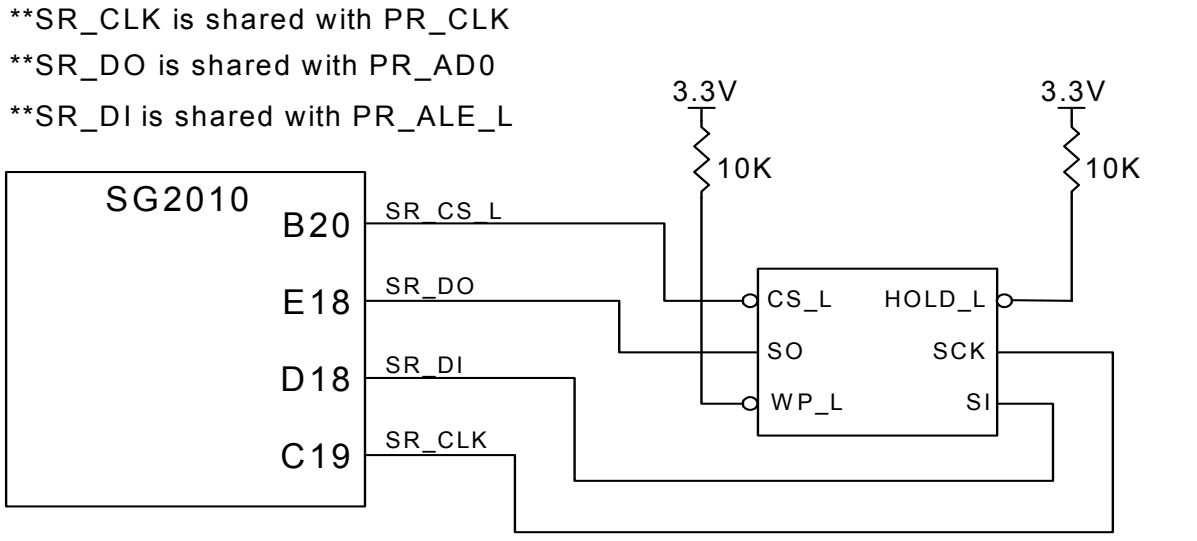
Serial ROM and Parallel ROM

6.1 Serial ROM

Many applications will utilize the SG2010 serial ROM (SROM) interface to preload SG2010 registers at reset time. For fabric native and distributed computing applications, SROM's are generally required. SROM's are typically used to setup BARs 2-5, which allow the establishment of fabric connections. SROM's are also recommended for PCI legacy applications where the fabric topology is large. In larger legacy topologies it may be desirable to hide the SG2010 Gateway function (not used in purely legacy environments) to alleviate any IO resource issues. For more information on the SROM interface see Section 3.18.3 on the SG2010 Hardware Reference Manual.

Since the SROM interface is slow (typically 1Mhz) there are no special layout or implementation requirements. A high-frequency 0.1µF decoupling capacitor close to the power pin is recommended. An 8-pin, 3.3V device, such as an Atmel 25640A 8Kx8 serial EEPROM can be used for the serial ROM. Figure 6–1 provides an example SROM circuit.

Figure 6–1 Serial ROM Circuit



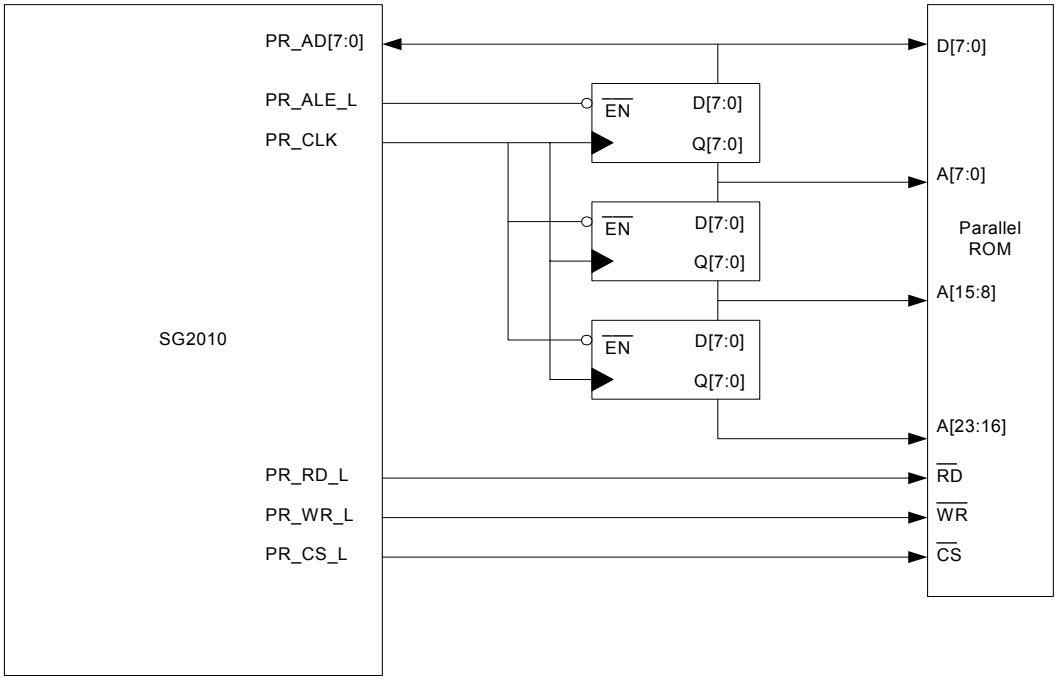
6.2 Parallel ROM

Note: The use of the Parallel ROM interface is optional.

The parallel ROM interface consists of 8 shared address/data signals and 5 control signals. The control signals are PR_CS_L (chip select), PR_WR_L (write strobe), PR_RD_L (read strobe), PR_ALE_L (address latch enable), and PR_CLK (address latch clock). Some of these signals are shared with the serial ROM interface. The parallel ROM can be used to implement a PCI Expansion ROM including the PCI Vital Product Data (VPD) extended capability, self test, etc. Since parallel ROMs have separate address and data lines, external address latches need to be provided in addition to the ROM itself. Addresses are driven eight bits at a time in three consecutive clock cycles starting with the least significant bits. Therefore, up to 24 bits of address are supported enabling Flash ROMs up to 16Mbytes.

Devices using a 3.3V supply such as the Intel 28F016S3, a 2Mx8 Flash device and 74LVC377A latches can be used. An example circuit for the parallel ROM with external latches is shown in Figure 6–2.

Figure 6–2 Parallel ROM Circuit



If the Parallel ROM interface is not being used PR_AD1 should be pulled to GND. PR_RD_L, PR_CS_L, and PR_WR_L can be left as NO CONNECTS and PR_AD[2:7] should be pulled appropriately (See Section 5.2 for more details).

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EMC Considerations

7.1 EMI Considerations

StarFabric links are based on Low Voltage Differential Signaling (LVDS) technology. Therefore, all emissions that are common mode or single ended are superfluous. Data collected on our reference board designs indicate the emissions at 622 Mhz (and its harmonics) are the main cause of concern.

There are generally two major ways to reduce emissions, shielding and filtering. We have reviewed our reference designs with industry leading EMC consultants and have developed the following recommendations:

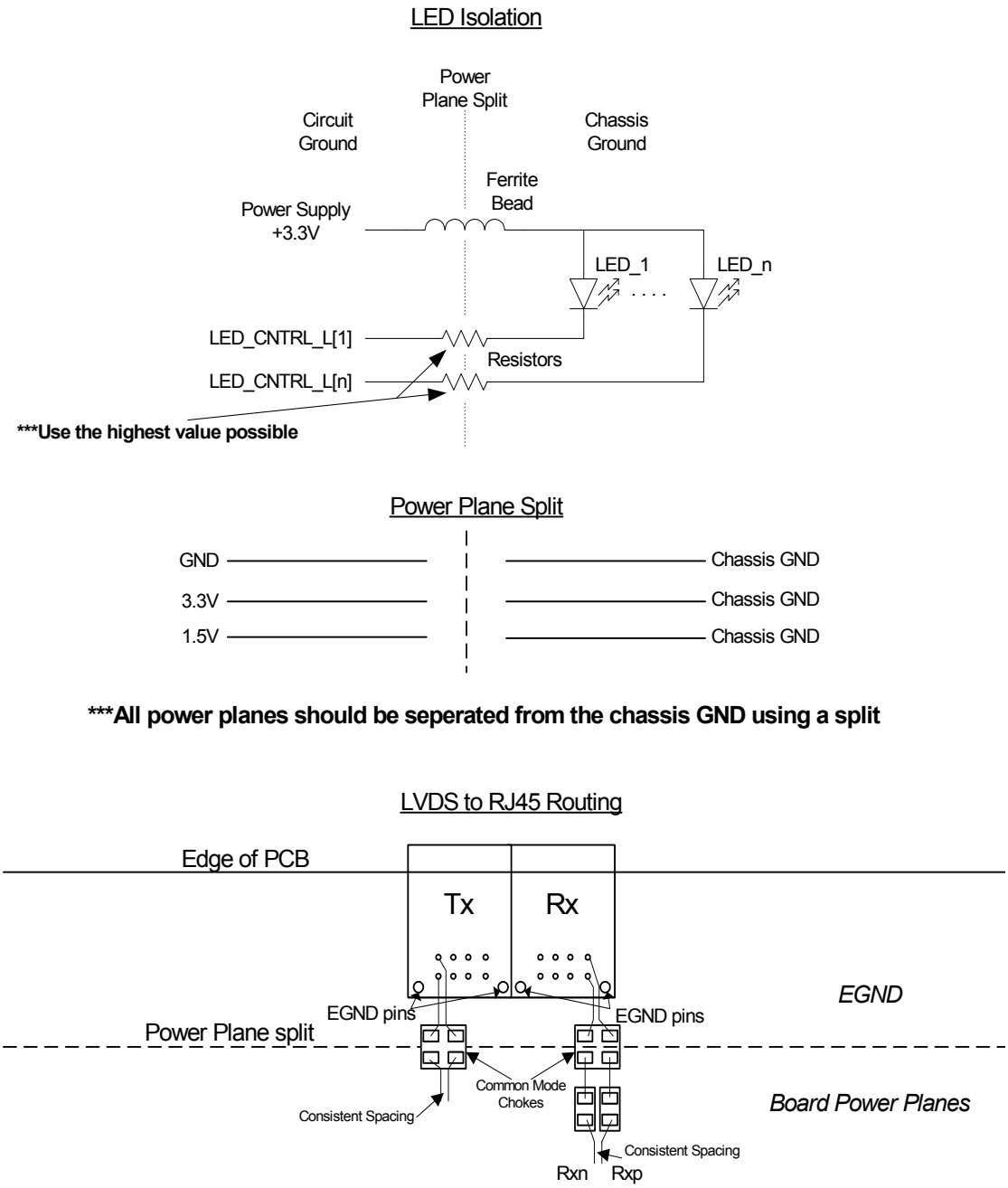
- High quality shielded CAT5E cable assemblies reduce emissions substantially if used in conjunction with shielded modular connectors. The shielded modular connectors should be connected to chassis ground via a low inductance path.
- Use etch layout techniques such as plane splits to reduce the amount of radiation from the “noisy” planes to the “quiet” chassis ground. Crossing the splits with only the LVDS signals is desirable. Also, if there are any sharp edge on the plane splits they should be chamfered (~45 degrees) to prevent antennas.
- Tightly matched etch lengths on differential pairs to reduce imbalance of the differential signal. Any imbalance becomes common mode noise and is most prevalent at multiples of 622Mhz.
- Chamfer the sharp edges of the LVDS traces to remove any antennae effect
- Add high frequency capacitors (.001uF) around the area where the LVDS traces are running. These capacitors are intended to suppress any high frequency noise that gets into the power/ground planes.
- Use gasketing around holes in the chassis to create a tighter RF seal.
- Use ferrite beads for LED’s placed on the chassis ground planes to filter out high frequencies from the “noisy” planes.
- Alternatively placing LEDs away from the chassis ground plane and using light pipes to conduct light to the edge panel.
- Use of common mode chokes on the transmit and receive LVDS pairs to filter out high frequency noise. (Impact on signal integrity should be assessed)

As a result of utilizing several of these EMI mitigation techniques StarGen's SFS2100 switch card and SGPCI64-A card met the following EMC emissions requirements:

EN 55022:1998 Class A ITE (EU)
FCC 47 CFR Part 15 Class A

Please see Figure 7–1 for an example implementation.

Figure 7–1 EMI Design Considerations



7.2 ESD Considerations

All electronic devices are subject to damage from ElectroStatic Discharge (ESD). There are precautions that should be taken with all such devices throughout the stages of development including device (chip) handling, PCB handling and installation, and during normal functional operation. StarFabric devices have been designed to withstand ESD events on all device pins. StarGen devices fully meet the ESD Charged-Body Model and Human-Body Model standards. In addition, StarGen boards and switches meet applicable system level standards. However, when designing boards and systems, designers should consider ESD as a possible threat especially if cable applications are being implemented.

There is a form of ESD associated with all links that use low loss cables such as Ethernet or CAT5E cables. The term Cable Discharge Event (CDE) is used to describe a statically charged cable being plugged into another device with resultant discharge and possible damage.

Shielded CAT5 or CAT5E cables, along with shielded connectors, are suggested as a good way to help prevent individual differential pair conductors from getting charged electrostatically.

Given the high speed low voltage nature of Starfabric links, it is important that any additional components that are used to protect the system from ESD be very low in capacitance so as not to adversely affect the link signal integrity during normal operation.

Stargen has experimented with devices such as Protek GBLC03 and found that they do provide additional protection and do not adversely affect link signal integrity.

ESD protection devices for cable applications should be placed near the cable connector. If AC coupling capacitors and the common mode chokes are used, the protection devices should be placed between them and the SG2010. The protection devices should have a solid low impedance connection to ground and they should be placed so that electrical stubs are minimized.

CompactPCI Hot Swap Requirements

8.1 CompactPCI Hot Swap Requirements

The SG2010 is designed to support the operation of CPCI boards as “Full Hot Swap,” as defined in the *CPCI Hot Swap Specification*. Operation as a “High Availability” platform requires vendor and application unique features that have been considered in the design of the SG2010 and StarFabric. When the SG2010 is used in a Hot Swap environment the following pins must be terminated appropriately:

- BDSEL_L (BGA location K3) - CompactPCI Hot Swap board seated. When sampled high, the SG2010 does not respond to or initiate any PCI transactions (after completing any ongoing transactions). When sampled low, the SG2010 responds to and initiates PCI transactions normally. This pin should be tied to ground by the backplane.
- L64EN_L (BGA location K2) - CompactPCI Hot Swap local 64-bit extension enable. When the SG2010 samples this signal low, it enables the PCI 64-bit extension signals. When the SG2010 samples this signal high, the PCI 64-bit extension signals are only enabled if REQ64_L is sampled low during RST_L or LRST_L. This pin should be pulled up (~100K) and tied to pin B5 of the CPCI J2 connector.
- LSTAT (BGA location J2) - CompactPCI Hot Swap ejector handle switch status. Sampled by the SG2010 to determine when the ejector handle switch is open or closed, controlling the hot swap state machine. When a “1”, the ejector handle is open. When a “0”, the ejector handle is closed. This pin should be pulled down with a 10K pulldown and tied to pin 1 of the ejector handle assembly through a 1K.
- ENUM_L (BGA location J4) - CompactPCI Hot Swap interrupt. The SG2010 can be enabled to sample this signal and forward it through the event dispatcher, and can be enabled to assert this signal when it receives an event directed to the ENUM_L EMU address. This pin should be pulled up (~100K) and tied to C25 of the CompactPCI J1 connector.
- SKIPINS/PR_AD[2] (BGA location E19) - When “1”, enables the hot swap controller to skip insertion state after power up. It does not effect re-insertion after removal. When “0', the hot swap controller goes through the insertion state as specified in the CompactPCI Hot Swap specification. The termination of this pin is dependent upon the application.

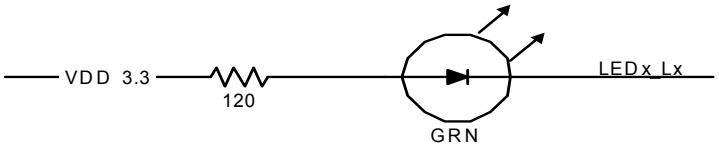
For more details on how to implement Hot Swap with the SG2010 please see the *CPCI Hot Swap Specification* and Section 3.10 of the SG2010 Hardware Reference Manual.

LED Usage

9.1 LED Overview

The SG2010 provides eight signal pins that can be used to drive external LEDs. These are LED0_L[3:0] and LED1_L[3:0]. The signals provide 24mA of sink and source current so that LEDs can be driven directly without the need for external drivers. The use of a current limiting resistor is recommended to ensure that the current flow is maintained below the 24mA limit.

Figure 9–1 Current Limiting Resistor



Two modes of operation are supported for the LED drive signals as follows:

1. Use of one LED for each differential pairstatus
2. Use of one LED for each StarGen link (four differential pairs) status.

The mode is selected at reset by sampling the PR_AD[3] signal (BGA location F18).

In addition to the use of LED signal pins for reporting link and differential pair status, direct control of LEDs with software is possible. Refer to the *SG2010 Hardware Reference Manual* for more information on software control of LEDs.

9.2 Use of One LED per LVDS Differential Pair

If the PR_AD[3] signal is sampled low at reset, the LEDx_L[3:0] signals are enabled to drive a logic "0" for each differential pair that is in the synchronized state with traffic enabled. The LEDx_L[3:0] signals will drive a “1” for each differential pair that is not in the synchronized state with traffic enabled.

If a differential pair is synchronized but traffic is not enabled for that differential pair, then the associated LEDx_L signal will toggle between a logic 1 and 0 with a frequency of approximately 500ms to blink the LED.

9.3 Use of One LED per StarGen Link

For some applications, the use of a single LED for a 4-differential pair link may be desired to reduce cost, power, and board real-estate. For these applications, the PR_AD[3] signal should be pulled high at reset.

When PR_AD[3] is sampled high at reset, the LEDx_L[0] signal is enabled to drive a logic "0" for each "link" that has at least one differential pair in the synchronized state with traffic enabled. The LEDx_L[0] signal will also drive a "1" for each "link" that is not in the synchronized state with traffic enabled.

If a "link" is synchronized but traffic is not enabled, then the associated LEDx_L[0] signal will toggle between a logic 1 and 0 with a period of approximately 500ms to blink the LED.

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Example Implementations

10.1 PCI Peripheral Card

If the SG2010 is going to be implemented on a PCI peripheral card all the system slot features including, the 2010 arbiter and central function features should be disabled. In addition, the 2010 should never be setup as a “leaf” with the bridge enabled because if placed in a fabric this is an illegal PCI configuration. When the 2010 is configured as a bridge enabled leaf device with central function enabled, its PCI interface acts like the secondary side of a bridge spawning a new PCI bus segment. In this configuration, the SG2010’s PCI interface cannot be connected to another PCI bus segment that is controlled by another host. The valid 2010 configurations for a PCI peripheral card implementation are “root” with bridge enabled/disabled and “leaf” with bridge disabled.

10.1.1 PCI Clock Routing

The PCI Specification requires that the PCI clock trace length is 2.5 +/- 0.1 inches for both 32-bit and 64-bit expansion boards. Also, the clock must only be routed to one load/device on the board. This loading restriction also applies to all shared PCI signals.

10.1.2 PCI Signal Routing

For the PCI 32-bit interface signals, the maximum trace length from the PCI device to the board's edge connector is 1.5 inches. For 64-bit extensions, the maximum trace length is 2 inches. The exceptions to these rules are interrupt signals, JTAG signals, and system signals (clock and reset). Shared PCI signal traces must have an unloaded characteristic impedance between 60 Ω and 100 Ω, with a propagation velocity between 150 and 190 picoseconds per inch.

10.1.3 Arbitration

The SG2010 should have its arbiter disabled. This is accomplished by putting a pull-down (~10K) on the PR_AD6 pin of the SG2010. Also, designers should take into account that the REQ_L0/AGNT_L (BGA loc M2) pin should connect to the GNT_L signal from the PCI connector and GNT_L0/AREQ_L (BGA loc M1) should connect to the REQ_L signal from the PCI connector. In addition the remaining REQ signals on the SG2010 should be pulled up using ~10K pull-ups.

10.1.4 Interrupts

The behavior of the interrupts depends on whether the SG2010 is setup as a Root or Leaf with Bridge Disabled. If setup as Root/Bridge Enabled the interrupts are outputs. All the interrupt pins of the SG2010 should be connected to the interrupts from the backplane. This will allow the Root SG2010 to assert the interrupts for the Leaf PCI buses. If the SG2010 is setup with the Bridge Disabled (Root or Leaf), the interrupts are local to the PCI bus and implementation will depend on the application. Also, for both Root and Leaf applications where a PCI connector is not used the IDSEL of the SG2010 should be connected to an address line according to the PCI Specification. Otherwise, the IDSEL signal should connect to the PCI connector's pin 26A.

10.1.5 Reset

The reset input pin RST_L of the SG2010 should connect to the reset from the PCI connector. The RSTO_L pin can be left as a no connect. The SG2010 should also have its central function feature disable by pulling down (~10K) the PR_AD7 pin.

10.2 PCI Expansion Backplane/PICMG System Slot Card

Designers interested in using the SG2010 for PCI expansion have 2 options; a PICMG system slot card or a custom PCI backplane that has an SG2010 on the planer. Both implementations require that the SG2010 be setup as a bridge enabled "leaf" device with its central function enabled. Refer to section 5.2 for the details on how to enable both the bridge and central functions. Designers interested in having multiple PCI segments can use a combination of SG2010's and StarGen's SG1010 switch chips. Please refer to the SG1010 Hardware Reference Manual and Hardware Implementation Guide for details on implementing an SG1010 design. When designing an SG2010 expansion backplane or PICMG system slot card there are several considerations that need to be made including; arbitration, reset, termination, and interrupts.

10.2.1 Arbitration

The SG2010 on an PICMG system slot card is expected to provide arbitration for all expansion slots capable of containing bus master cards. The SG2010 arbiter is capable of supporting 9 bus masters plus the SG2010 as a bus master. The SG2010 arbiter is enabled at reset time by pulling up (~10K) the PR_AD6 pin. If enabled the SG2010 REQ_L0/AGNT_L (BGA loc M2) is used as a REQ line and GNT_L0/AREQ_L (BGA loc M1) is used as a GNT line. The arbitration on a custom PCI backplane will vary based on the application. If another arbiter is used, the SG2010 arbiter should be disabled and GNT_L0/AREQ_L (BGA loc M1) should be used as a REQ line and REQ_L0/AGNT_L used as a REQ line. All SG2010 REQ signals should be pulled up in either Arbiter enabled or Arbiter disabled mode.

10.2.2 Termination

If designing a SG2010 PICMG system slot board or PCI expansion backplane pull-ups are required on the following signals: FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, INTA#, INTB#, INTC#, INTD#, REQ64#, ACK64#, AD[63:32], CBE#[3:7], and PAR64. Please see the PCI Specification for recommended pull-up values.

10.2.3 Reset

If the SG2010 is used on a PICMG system slot board it is responsible for driving PCI reset. An on board reset circuit, such as the Dallas Semiconductor power-on reset part DS1830AS, is required. Typically, the output of the DS1830 should connect to the 2010 RST_L input and the RSTO_L pin of the 2010 should connect to the PCI backplane. Connecting the RSTO_L pin to the backplane will allow a reset on the host system to propagate to the remote PCI bus. The reset circuit for a custom PCI backplane will vary based on the application.

10.2.4 Clocking

When the SG2010 is implemented on a PICMG system slot the board designer should provide PCI clocks to the appropriate connector pins for each backplane slot. These connector pins are specified in the PICMG PCI/ISA Passive Backplane Specification. Trace routing for the clock signals must be matched in length. To account for the maximum backplane skew, the etch from the clock buffer to the SG2010 CLK BGA pin should be approximately 8 inches longer than the etch from the clock buffers to the PCI connector. The clocking scheme on a custom PCI expansion backplane will vary based on application. The principle for PCI clocking is to have the PCI clock signal arrive at each device on the bus segment at the same time. Backplane skew of the clock signal needs to be accounted for, especially for 66 Mhz operation.

10.2.5 Interrupts

When the SG2010 is in a system slot with the PCI Bridge Function enabled the INT signals are inputs. Designers should be aware that in order for the SG2010 to detect a clean transition, the signal transition time between 1.45 and 1.85V should be a maximum of 4 PCI clock cycles. When an interrupt is signaled on the Leaf PCI bus, the SG2010 forwards the interrupt as a StarFabric event frame to the Root SG2010. The Root SG2010, in turn, asserts the appropriate INT line. The interrupts on the backplane should be routed according to the PCI to PCI Bridge Architecture Specification (this is commonly known as interrupt swizzling). If the bridge function is disabled, the interrupts are local to the Leaf PCI bus and their behavior can be programmed through software.

10.3 CompactPCI

The SG2010 can be used on either a system or peripheral slot CompactPCI board. There are several considerations that need to be made when building either board type, including arbitration, termination, clocking, reset and interrupts. Also, there are a few requirements that apply to both board types. These requirements are outlined below:

- The following PCI bussed signals require 10 Ohm (+-5%) series resistors: AD0:31, CBE#0-3, PAR, FRAME#, IRDY#, TRDY#, STOP#, LOCK#, IDSEL, DEVSEL#, PERR#, SERR#, and RST#. In addition INTA#, INTB#, INTC#, INTD#, AD32-64, CBE#4-7, REQ64#, ACK64# and PAR64 require termination resistors if used on the board.
- Trace impedance must be 65Ω +/-10%.
- Signal trace lengths must not exceed 2.5 inches for both 32-bit and 64-bit boards. This length is the distance from the CompactPCI connector to the SG2010 PCI device pin, including any series termination resistors. System slot boards can also have an additional PCI load on them.

For more details please refer to the CompactPCI PICMG 2.0 D3.0 Specification.

10.3.1 CompactPCI System Slot Requirements

When designing an SG2010 system slot board, the designer should take into account that the board needs to provide clocks, arbitration, and termination. Also, the SG2010 should always be setup as a “Leaf” device with its central function enabled. Refer to section 5.2 for details on how to configure these features.

10.3.1.1 Clocking

When the SG2010 PCI interface is connected to CPCI J1/J2 on a CompactPCI system slot card, the board designer should provide PCI clocks to the appropriate J1/J2 connector pins for each backplane slot. These connector pins are specified in the *CompactPCI Specification*, Tables 15 and 16. Trace routing for the clock signals must be matched in length. The electrical length of series termination should be included in the trace length calculation. To account for the maximum backplane skew (1.2 ns), the etch from the clock buffer to the SG2010 CLK BGA pin should be approximately 7 inches (assuming 170 ps/in) longer than the etch from the clock buffers to the CPCI connector.

10.3.1.2 Arbitration

If the SG2010 PCI interface is used in a CompactPCI system slot it is required to provide arbitration. To enable the arbitration function of the SG2010, PR_AD6 must be pulled up with ~10 K resistor. When the arbiter is enabled on the SG2010, REQ_L0/AGNT_L (BGA loc M2) is used as a REQ line and GNT_L0/AREQ_L (BGA loc M1) is used as a GNT line. All SG2010 REQ signals should be pulled up with a 100 K pullup.

10.3.1.3 Termination

According to the CompactPCI specification, system slot boards are required to provide pull-ups on the following signals: FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, INTA#, INTB#, INTC#, INTD#, REQ64#, ACK64#, AD[63:32], CBE#[4:7], and PAR64. The required pull-up values depend on the signaling environment and loading. Assuming 9 loads, the pull-up value should be 1K (+-5%) for 5V and 2.7K (+-5%) for 3.3V.

In addition to the pull-ups listed above, the SG2010 Req signals require 100 KOhm pull-ups and the IDSEL input to the SG2010 should be pulled down using a ~10K pull-down. Also, each clock signal and GNT arbitration signal require series termination resistors.

10.3.1.4 Interrupts

When the SG2010 is in a system slot with the Bridge enabled the INT signals are inputs and are constantly sampled. Designers should be aware that in order for the SG2010 to detect a clean transition, the signal transition period between 1.45 and 1.85V should be a maximum of 4 PCI clock cycles. When an interrupt is asserted or deasserted on the CompactPCI bus, the SG2010 forwards an event frame to the Root SG2010. The Root SG2010 in turn asserts the appropriate INT line. The interrupts on the backplane should be connected to the associated interrupt on the SG2010: INTA-INTA ... INTD-INTD.

10.3.1.5 Reset

If the SG2010 is interfacing to a CompactPCI system slot, it is responsible for driving reset. An on board reset circuit is required for a system slot implementation. The Dallas Semiconductor Power-On reset part DS1830AS has been used in past designs. Typically, the output of the DS1830 should connect to the 2010 RST_L input and the RSTO_L pin of the 2010 should connect to the backplane. Connecting the RSTO_L pin to the backplane will allow a remote system host to reset the CompactPCI bus.

10.3.2 CompactPCI Peripheral Slot Requirements

When designing an SG2010 peripheral slot board there are several considerations that the designer should consider, including clock routing, termination, reset, interrupts, and arbitration. When setup in a peripheral slot the 2010 can be either a Root (Bridge Enabled or Gateway Only) or a Leaf Gateway Only, and its central function should be disabled. Refer to section 5.2 for details on how to configure these features.

10.3.2.1 Clock Routing

According to the CompactPCI specification the PCI clock signal trace length from J1 to the SG2010 must be 2.5 +/-0.1 inches. Also, the trace is limited to driving only one load.

10.3.2.2 Arbitration

When used in a peripheral slot application the SG2010 should have its arbiter disabled. This is accomplished by putting a pull-down (~10K) on the PR_AD6 pin of the SG2010. Also, designers should take into account that the REQ_L0/AGNT_L (BGA loc M2) pin should connect to the GNT_L signal from J1 and GNT_L0/AREQ_L (BGA loc M1) should connect to the REQ_L signal from J1. In addition the remaining REQ signals on the SG2010 should be pulled up using ~10K pull-up.

10.3.2.3 Termination

Only one load is allowed per PCI signal on a peripheral board.

10.3.2.4 Interrupts

The behavior of the interrupts depend on whether the SG2010 is setup as a Root or Leaf. If setup as a Root the interrupts are outputs. All the interrupt pins of the SG2010 should be connected to the interrupts from the backplane. This will allow the Root SG2010 to assert the interrupts signaled by device on the Leaf PCI buses on the system host.

10.3.2.5 Reset

The reset input pin RST_L of the SG2010 should connect to the reset from J1. The RSTO_L pin can be left as a no connect.

10.3.3 CompactPCI Mixed System/Peripheral Slot Requirements

A design goal for an SG2010 CompactPCI board may be the ability to use the board in either a System Slot or a Peripheral slot. This requires a flexible design that enables and disables features based on the slot type. These features include central function responsibility (reset generation, 64-bit initialization, arbitration, clock source/receive, termination, and etch length/routing rules. The selection of System slot or peripheral slot can be manual (via switches, jumpers, etc.) or automatic (via FETs, etc.). Extreme care must be exercised both in the design and the use of boards that can be plugged into either peripheral or system slots.

10.3.3.1 Clock Routing

Clocks need to be inputs and of specific lengths in peripheral slots. They need to be outputs and carefully routed and matched in system slots. When used in a system slot, an external clock buffer such as a TI CDC351 is required to generate clocks for each peripheral slot and the onboard SG2010. Also, a FET switch is required for both the SG2010 PCI clock and the clock to J1. In a peripheral slot the J1 PCI clock should connect to the SG2010 clock. In a system slot both the J1 PCI clock and the SG2010 should connect to an individual output from the clock buffer.

10.3.3.2 Arbitration

Typically, when an SG2010 board is being plugged into a peripheral slot, the arbiter will be disabled and the SG2010 will not be setup as central function (The main processor board generally provides arbitration and performs central functions). When in a system slot, an SG2010 board will normally be setup with central function and arbiter enabled. To enable both the arbiter and central function, the PRAD6 and PRAD7 signals must be pulled high. To disabled both, they should be pulled low. See Section 5.2 for more information on these and other SG2010 reset strap options. Arbitration for the CPCI bus using REQ/GNT requires that these two signals are output/input, respectively, in a peripheral slot. In a system slot, all of the REQ/GNT pairs become input/output. FETS can be used to control how the GNT and REQ lines are connected. For CPCI, the sysen_l pin (J2 pin C2) can be used as the input to the FETS to control how the REQ and GNT lines are connected. When in a peripheral slot, the CPCI GNT_L signal (J1 pin E5) should be connected to the SG2010 REQ_L0 input (BGA location M2), and the CPCI REQ_L (J1 pin A6) signal must be connected to the SG2010

GNT_L0 output (BGA location M1). When in a system slot, the SG2010 board must connect SG2010 REQ_L[0:8] to the CPCI REQ_L[0:8] and SG2010 GNT_L[0:8] to CPCI GNT_L[0:8].

10.3.3.3 Reset

On a mixed system/peripheral slot board, the Reset and IDSEL signals must also be able to be switched. The 2010 reset must connect to an on board reset circuit in a system slot and to the J1 RST_L in a peripheral slot. The J1 reset must connect to the RSTO_L pin of the SG2010 in a system slot environment.

10.3.3.4 Termination

A system/peripheral slot board must be able to "switch in" the required ~2.7 K pull-ups for system slot application and "switch out" the pull-ups in a peripheral slot.

10.4 SG2010 PMC Card

If the 2010 is implemented on a PMC card it should follow all the rules defined in the IEEE P1386.1 PMC ("PCI Mezzanine Card") standard. This specification requires that the SG2010 always be terminated to disable its system slot features including, the 2010 arbiter and central function features. In addition, the 2010 should never be setup as a "leaf" with bridge enabled because this is an illegal PCI configuration. The valid 2010 configurations for a PMC card implementation are "root" with bridge enabled/disabled and "leaf" with bridge disabled.

10.4.1 PCI Clock Routing

The PCI Specification requires that the PCI clock trace length is 2.5 +/- 0.1 inches for both 32-bit and 64-bit expansion boards. Also, the clock must only be routed to one load/device on the board. This loading restriction also applies to all shared PCI signals.

10.4.2 Arbitration

The SG2010 should have its arbiter disabled. This is accomplished by putting a pull-down (~10K) on the PR_AD6 pin of the SG2010. Also, designers should take into account that the REQ_L0/AGNT_L (BGA loc M2) pin should connect to the GNT_L signal from the PCI connector and GNT_L0/AREQ_L (BGA loc M1) should connect to the REQ_L signal from the PCI connector. In addition the remaining REQ signals on the SG2010 should be pulled up using ~10K pull-ups.

10.4.3 Interrupts

The behavior of the interrupts depends on whether the SG2010 is setup as a Root or Leaf with Bridge Disabled. If setup as Root/Bridge Enabled the interrupts are outputs. All the interrupt pins of the SG2010 should be connected to the interrupts from the backplane. This will allow the Root SG2010 to assert the interrupts for the Leaf PCI buses. If the SG2010 is setup with the Bridge Disabled (Root or Leaf), the interrupts are

local to the PCI bus and implementation will depend on the application. Also, for both Root and Leaf mode, the idsel of the SG2010 should be connected to an address line according to the PCI Specification.

10.4.4 Reset

The reset input pin RST_L of the SG2010 should connect to the reset from the PCI connector. The RSTO_L pin can be left as a no connect. The SG2010 should also have its central function feature disable by pulling down (~10K) the PR_AD7 pin.

STARGEN 11

Common Implementation Issues

11.1 Common Implementation Issues

The following is a list of the most common implementation issues experienced with SG2010 designs.

1. Improper connection of the SG2010 REQ_0 and GNT_0 signals. Please see Chapter 10 for details on how to route Arbiter signals based on the implementation requirements.
   - If the SG2010 Arbiter is enabled (PR_AD6 is pulled up), REQ_0 (BGA location M2) should be used as an SG2010 REQ signal and GNT_0 (BGA location M1) should be used as an SG2010 GNT signal.
   - If the SG2010 Arbiter is disabled (PR_AD6 is pulled up), REQ_0 (BGA location M2) should connect to the GNT signal from the connector and GNT_0 (BGA location M1) should connect to the REQ signal.
2. Improper routing of the LVDS signals (See Section 3.3)
   - Signals not routed differentially for the entire length of run. Often split near connectors.
   - The positive and negative signal that comprise a differential pair must be routed on the same layer
   - LVDS signals routed to close to non-LVDS signals
   - LVDS pairs routed to close to other LVDS pairs
   - Skew not matched correctly between the positive and negative signals of an LVDS pair
3. Noise on Analog 1.5 V supply pins
   - Supply not derived close to the SG2010 BGA
   - High-frequency decoupling capacitor not placed close to the SG2010 BGA
   - Choke circuit not implemented to isolate Analog supply from digital supply noise
4. Incorrect inductor used for supply choke circuits

- Careful attention should be taken when selecting the inductors for the supply choke circuits. The inductors must be able to handle the current requirements for the supply

5. Termination (Chapter 5)
   - Testmode[0:3] not pulled down
   - INTA-D termination
   - IDSEL not pulled down for the SG2010 LEAF/Bridge Enabled configuration
   - REQ[1:8] not pulled-up when the SG2010 arbiter is disabled

6 Hot Swap issues for CompactPCI implementation
   - BDSEL_L and LSTAT should be pulled down for normal operation.
   - SKIPINS (PR_AD2) should be pulled high for normal operation.

7 INT swizzle (PICMG vs. PCI)
   - The PCI interrupt swizzle for a PICMG backplane is different then the PCISIG standard PCI-to-PCI bridge specification. Please see the PCI to PCI Bridge Architecture Specification Rev 1.2 and PICMG 1.0 specification for more details. The SG2010 conforms to the PCI specification.

8. Leaf SG2010 Interrupt filter circuit
   - The interrupt signal transition period for an interrupt on a Leaf SG2010 PCI bus must be a maximum of 4 PCI clock cycles to assure clean detection by the SG2010.

9. In legacy PCI application the reset of the Root SG2010 is deasserted before the reset of the Leaf SG2010.

Glossary

BGA	Ball Grid Array
BRIDGE	An edge node that provides protocol translation; for example, a bridge between the fabric and a PCI bus.
CMOS	Complementary Metal-Oxide Semiconductor
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read-Only Memory
GPIO Signals	General Purpose I/O Signals
LED	Light-Emitting Diode
LVDS	Low Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PICMG	PCI Industrial Computer Management Group
PLL	Phase Lock Loop
PROM	Programmable Read-Only Memory
PCB	Printed Circuit Board
ROM	Read-Only Memory
SBC	Single Board Computers
SROM	Serial Read-Only Memory
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
TTL	Transistor Transistor Logic